WHAT IS CLAIMED IS:

1. A clock data recovery circuit to be used in the SONET/SDH, comprising:

a clock extracting part for extracting an input clock from an input signal;

a retiming clock generating part for generating a retiming clock for retiming said input signal;

a first-in first-out memory part for temporarily storing the retimed input signal; and

a phase adjusting part for preventing coincidence of a writing side address value and a reading-out side address value by controlling writing timings at the first-in first-out memory part by said retiming clock and controlling reading-out timings by said input clock.

2. The clock data recovery circuit according to Claim 1, wherein said clock extracting part comprises:

a first phase comparator circuit which outputs an up signal or down signal by comparing the phase of said retiming clock and the phase of said input signal, and outputs said input signal after retiming it by the retiming clock;

a first up/down counter which outputs a count value added or subtracted by 1 in accordance with the up signal or down signal outputted from said first phase comparator circuit;

a weighting circuit which outputs an up signal or down signal that has been weighted by the count value inputted from the first up/down counter;

a voltage value determining part which determines and outputs a voltage value based on the up signal or down signal inputted from the weighting circuit; and

a voltage controlled oscillator circuit which outputs said input clock by determining the oscillation frequency in accordance with the voltage value inputted from the voltage value determining part.

3. The clock data recovery circuit according to Claim 2, wherein said retiming clock generating part comprises:

a second up/down counter which outputs a count value added or subtracted by 1 in accordance with the up signal or down signal inputted from the first phase comparator circuit; and

a phase switching circuit which outputs said retiming clock by adjusting the phase of said input clock inputted from the clock extracting part by the count value inputted from the second up/down counter.

4. The clock data recovery circuit according to Claim 2, wherein said weighting circuit comprises:

a magnitude comparator for comparing the up signal or down signal inputted from the first up/down counter and a fixed value; and

a logical circuit which determines a signal to be outputted to the voltage value determining part based on magnitude comparison data from said magnitude comparator, the count value from the first up/down counter, and the count value inputted from the third up/down counter.

5. The clock data recovery circuit according to Claim

3, wherein said weighting circuit comprises:

a magnitude comparator for comparing the up signal or down signal inputted from the first up/down counter and a fixed value; and

a logical circuit which determines a signal to be outputted to the voltage value determining part based on magnitude comparison data from said magnitude comparator, the count value from the first up/down counter, and the count value inputted from the third up/down counter.

6. The clock data recovery circuit according to Claim 2, wherein said phase adjusting part comprises:

a first counter which outputs a count value counted at the timings of said retiming clock inputted from said retiming clock generating part and the highest-order bit of this count value;

a second counter which outputs a count value counted at the timings of said input clock inputted from said clock extracting part and the highest-order bit of this count value;

a second phase comparator circuit which outputs an up signal or down signal by comparing the phase of the highest-order bit of the count value inputted from the first counter and the phase of the highest-order bit of the count value inputted from the second counter; and

a third up/down counter which outputs a count value added or subtracted by 1 in accordance with the up signal or down signal inputted from said second phase comparator circuit.

7. The clock data recovery circuit according to Claim 3, wherein said phase adjusting part comprises:

a first counter which outputs a count value counted at the timings of said retiming clock inputted from said retiming clock generating part and the highest-order bit of this count value;

a second counter which outputs a count value counted at the timings of said input clock inputted from said clock extracting part and the highest-order bit of this count value;

a second phase comparator circuit which outputs an up signal or down signal by comparing the phase of the highest-order bit of the count value inputted from the first counter and the phase of the highest-order bit of the count value inputted from the second counter; and

a third up/down counter which outputs a count value added or subtracted by 1 in accordance with the up signal or down signal inputted from said second phase comparator circuit.

8. The clock data recovery circuit according to Claim 2, wherein said first phase comparator circuit comprises:

a first flip-flop which retimes said input signal by said retiming clock and then outputs it;

a second flip-flop which outputs a high signal or low signal by comparing the phase of said input signal and the phase of said retiming clock; and

a third flip-flop which outputs an up signal or down signal in accordance with the high signal or low signal

inputted from said second flip-flop.

9. The clock data recovery circuit according to Claim 3, wherein said first phase comparator circuit comprises:

a first flip-flop which retimes said input signal by said retiming clock and then outputs it;

a second flip-flop which outputs a high signal or low signal by comparing the phase of said input signal and the phase of said retiming clock; and

a third flip-flop which outputs an up signal or down signal in accordance with the high signal or low signal inputted from said second flip-flop.

10. The clock data recovery circuit according to Claim 4, wherein said first phase comparator circuit comprises:

a first flip-flop which retimes said input signal by said retiming clock and then outputs it;

a second flip-flop which outputs a high signal or low signal by comparing the phase of said input signal and the phase of said retiming clock; and

a third flip-flop which outputs an up signal or down signal in accordance with the high signal or low signal inputted from said second flip-flop.

11. The clock data recovery circuit according to Claim 5, wherein said first phase comparator circuit comprises:

a first flip-flop which retimes said input signal by said retiming clock and then outputs it;

a second flip-flop which outputs a high signal or low

signal by comparing the phase of said input signal and the phase of said retiming clock; and

a third flip-flop which outputs an up signal or down signal in accordance with the high signal or low signal inputted from said second flip-flop.

12. The clock data recovery circuit according to Claim 6, wherein said first phase comparator circuit comprises:

a first flip-flop which retimes said input signal by said retiming clock and then outputs it;

a second flip-flop which outputs a high signal or low signal by comparing the phase of said input signal and the phase of said retiming clock; and

a third flip-flop which outputs an up signal or down signal in accordance with the high signal or low signal inputted from said second flip-flop.

13. The clock data recovery circuit according to Claim 7, wherein said first phase comparator circuit comprises:

a first flip-flop which retimes said input signal by said retiming clock and then outputs it;

a second flip-flop which outputs a high signal or low signal by comparing the phase of said input signal and the phase of said retiming clock; and

a third flip-flop which outputs an up signal or down signal in accordance with the high signal or low signal inputted from said second flip-flop.